LExxAB
LExxC

Very low dropout voltage regulators with inhibit function

Datasheet — production data

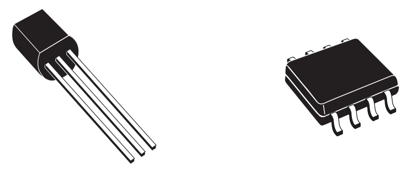
Features

- Very low dropout voltage (0.2 V typ.)
- Very low quiescent current (typ. 50 µA in OFF mode, 0.5 mA in ON mode, no load)
- Output current up to 100 mA
- Output voltages of 3 V, 3.3 V, 4.5 V, 5 V, 8 V
- Internal current and thermal limit
- Small 2.2 µF capacitor for stability
- Available in ± 1% (A) or ± 2% (C) selection at 25 °C
- Supply voltage rejection: 80 dB (typ.)
- Temperature range: - 40 to 125 °C

Description

The LExxAB and LExxC are very low dropout voltage regulators available in SO-8 and TO-92 packages and over a wide range of output voltages.

The very low dropout voltage (0.2 V) and the very low quiescent current make them particularly suitable for low-noise low-power applications and especially in battery-powered systems.



These devices are pin-to-pin compatible with the older L78Lxx series. Furthermore, in the 8-pin configuration (SO-8) they employ a shutdown logic control (pin 5, TTL compatible). This means that when the device is used as a local regulator, a part of the board can be put in standby, decreasing even more total power consumption. In the three-terminal configuration (TO-92) the device is always in the ON state, maintaining the same electrical performance. It requires only a 2.2 µF capacitor for stability, reducing component size and cost.

Table 1. Device summary

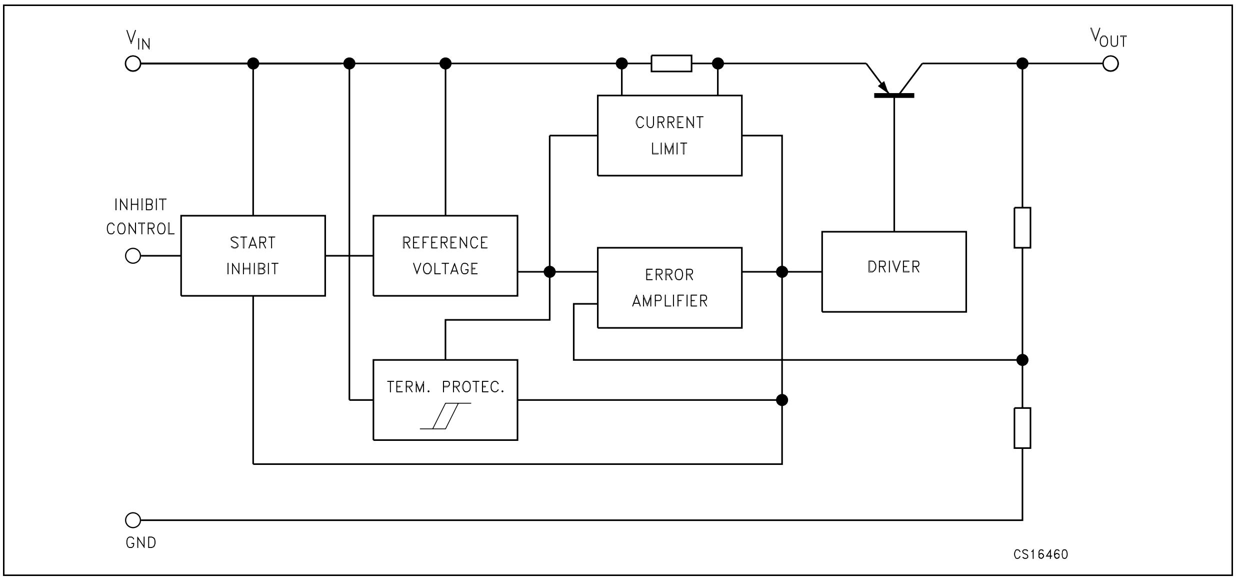
Order codes			Output voltages
SO-8 (tape and reel)	TO-92 (tape and reel)	TO-92 (Ammopak)	
	LE30ABZ-TR		3 V
LE30CD-TR			3 V
LE33CD-TR	LE33CZ-TR	LE33CZ-AP	3.3 V
LE45CD-TR			4.5 V
LE50ABD-TR		LE50ABZ-AP	5 V
LE50CD-TR			5 V
LE80CD-TR			8 V

This is information on a product in full production.

Contents

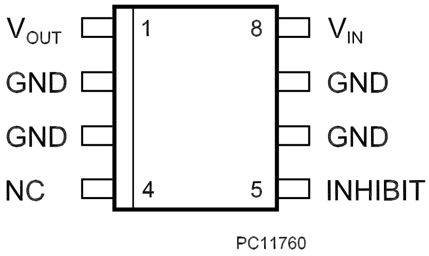
1 Diagram

Figure 1. Block diagram

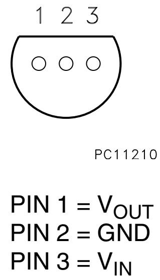


2 Pin configuration

Figure 2. Pin connections (top view for SO-8, bottom view for TO-92)



SO-8



TO-92

3 Maximum ratings

Table 2. Absolute maximum ratings

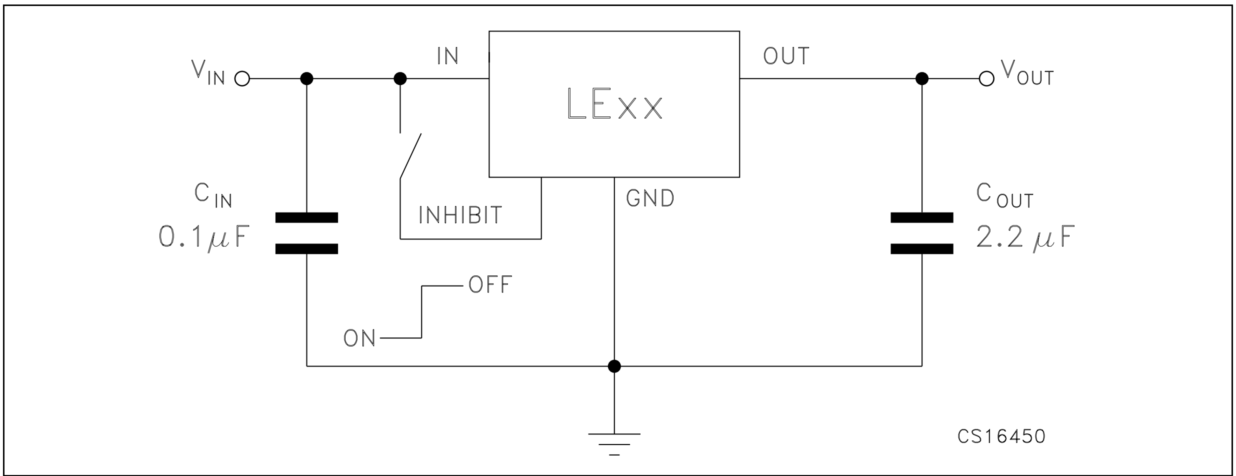
Symbol	Parameter	Value	Unit
V_I	DC input voltage	20	V
I_O	Output current	Internally limited (1)	
P_{TOT}	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	-65 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

1. Our SO-8 package used for voltage regulators is modified internally to have pins 2, 3, 6 and 7 electrically fused to the die attach pad. This particular frame decreases the total thermal resistance of the package and increases its ability to dissipate power when an appropriate area of copper on the printed circuit board is available for heatsinking. The external dimensions are the same as for the standard SO-8.

Table 3. Thermal data

Symbol	Parameter	SO-8	TO-92	Unit
R_{thJC}	Thermal resistance junction-case	20		°C/W
R_{thJA}	Thermal resistance junction-ambient	55	200	°C/W

Figure 3. Test circuit



Note: If the INHIBIT pin is left floating, the regulator is in the ON mode. However, to avoid picking up any noise, it is suggested to ground it when the Inhibit function is not used.

4 Electrical characteristics

Refer to the test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified.

Table 4. Electrical characteristics for LE30AB

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 5 V		2.970	3	3.030	V
		I_O = 10 mA, V_I = 5 V, T_J = -25 to 85°C		2.940		3.060	
V_I	Operating input voltage	I_O = 100 mA				18	V
I_O	Output current limit			150			mA
ΔV_O	Line regulation	V_I = 3.7 to 18 V, I_O = 0.5 mA			3	15	mV
ΔV_O	Load regulation	V_I = 4 V, I_O = 0.5 to 100 mA			3	15	mV
I_d	Quiescent current	V_I = 4 to 18 V, I_O = 0 mA	ON mode		0.5	1	mA
		V_I = 4 to 18 V, I_O = 100 mA			1.5	3	
		V_I = 6 V	OFF mode		50	100	µA
SVR	Supply voltage rejection	I_O = 5 mA, V_I = 5 ± 1 V	f = 120 Hz		81		dB
			f = 1 kHz		76		
			f = 10 kHz		60		
eN	Output noise voltage	B = 10 Hz to 100 kHz			50		µV
V_d	Dropout voltage	I_O = 100 mA			0.2	0.4	V
		I_O = 100 mA, T_J = -40 to 125°C				0.5	
V_{IL}	Control input logic low	T_J = -40 to 125°C				0.8	V
V_{IH}	Control input logic high	T_J = -40 to 125°C		2			V
I_I	Control input current	V_I = 6 V, V_C = 6 V			10		µA
C_O	Output bypass capacitance	ESR = 0.1 to 10 Ω, I_O = 0 to 100 mA		2	10		µF

Refer to the test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified.

Table 5. Electrical characteristics for LE30C

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 5 V		2.940	3	3.060	V
		I_O = 10 mA, V_I = 5 V, T_J = -25 to 85°C		2.880		3.120	
V_I	Operating input voltage	I_O = 100 mA				18	V
I_O	Output current limit			150			mA
ΔV_O	Line regulation	V_I = 3.7 to 18 V, I_O = 0.5 mA			3	20	mV
ΔV_O	Load regulation	V_I = 4 V, I_O = 0.5 to 100 mA			3	25	mV
I_d	Quiescent current	V_I = 4 to 18 V, I_O = 0 mA	ON mode		0.5	1	mA
		V_I = 4 to 18 V, I_O = 100 mA			1.5	3	
		V_I = 6 V	OFF mode		50	100	µA
SVR	Supply voltage rejection	I_O = 5 mA, V_I = 5 ± 1 V	f = 120 Hz		81		dB
			f = 1kHz		76		
			f = 10 kHz		60		
eN	Output noise voltage	B = 10 Hz to 100 kHz			50		µV
V_d	Dropout voltage	I_O = 100 mA			0.2	0.4	V
		I_O = 100 mA, T_J = -40 to 125°C				0.5	
V_{IL}	Control input logic low	T_J = -40 to 125°C				0.8	V
V_{IH}	Control input logic high	T_J = -40 to 125°C		2			V
I_I	Control input current	V_I = 6 V, V_C = 6 V			10		µA
C_O	Output bypass capacitance	ESR = 0.1 to 10 Ω, I_O = 0 to 100 mA		2	10		µF

Refer to the test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified.

Table 6. Electrical characteristics for LE33C

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 5.3 V		3.234	3.3	3.366	V
		I_O = 10 mA, V_I = 5.3 V, T_J = -25 to 85°C		3.168		3.432	
V_I	Operating input voltage	I_O = 100 mA				18	V
I_O	Output current limit			150			mA
ΔV_O	Line regulation	V_I = 4 to 18 V, I_O = 0.5 mA			3	20	mV
ΔV_O	Load regulation	V_I = 4.3 V, I_O = 0.5 to 100 mA			3	25	mV
I_d	Quiescent current	V_I = 4.3 to 18 V, I_O = 0 mA	ON mode		0.5	1	mA
		V_I = 4.3 to 18 V, I_O = 100 mA			1.5	3	
		V_I = 6 V	OFF mode		50	100	µA
SVR	Supply voltage rejection	I_O = 5 mA, V_I = 5.3 ± 1 V	f = 120 Hz		80		dB
			f = 1 kHz		75		
			f = 10 kHz		60		
eN	Output noise voltage	B = 10 Hz to 100 kHz			50		µV
V_d	Dropout voltage	I_O = 100 mA			0.2	0.4	V
		I_O = 100 mA, T_J = -40 to 125°C				0.5	
V_{IL}	Control input logic low	T_J = -40 to 125°C				0.8	V
V_{IH}	Control input logic high	T_J = -40 to 125°C		2			V
I_I	Control input current	V_I = 6 V, V_C = 6 V			10		µA
C_O	Output bypass capacitance	ESR = 0.1 to 10 Ω, I_O = 0 to 100 mA		2	10		µF

Refer to the test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified.

Table 7. Electrical characteristics for LE45C

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 6.5 V		4.41	4.5	4.59	V
		I_O = 10 mA, V_I = 6.5 V, T_J = -25 to 85°C		4.32		4.68	
V_I	Operating input voltage	I_O = 100 mA				18	V
I_O	Output current limit			150			mA
ΔV_O	Line regulation	V_I = 5.2 to 18 V, I_O = 0.5 mA			4	30	mV
ΔV_O	Load regulation	V_I = 5.5 V, I_O = 0.5 to 100 mA			3	25	mV
I_d	Quiescent current	V_I = 5.5 to 18 V, I_O = 0 mA	ON mode		0.5	1	mA
		V_I = 5.5 to 18 V, I_O = 100 mA			1.5	3	
		V_I = 6 V	OFF mode		50	100	µA
SVR	Supply voltage rejection	I_O = 5 mA, V_I = 6.5 ± 1 V	f = 120 Hz		77		dB
			f = 1 kHz		72		
			f = 10 kHz		60		
eN	Output noise voltage	B = 10 Hz to 100 kHz			50		µV
V_d	Dropout voltage	I_O = 100 mA			0.2	0.4	V
		I_O = 100 mA, T_J = -40 to 125°C				0.5	
V_{IL}	Control input logic low	T_J = -40 to 125°C				0.8	V
V_{IH}	Control input logic high	T_J = -40 to 125°C		2			V
I_I	Control input current	V_I = 6 V, V_C = 6 V			10		µA
C_O	Output bypass capacitance	ESR = 0.1 to 10 Ω, I_O = 0 to 100 mA		2	10		µF

Refer to the test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified.

Table 8. Electrical characteristics for LE50AB

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 7 V		4.95	5	5.05	V
		I_O = 10 mA, V_I = 7 V, T_J = -25 to 85°C		4.9		5.1	
V_I	Operating input voltage	I_O = 100 mA				18	V
I_O	Output current limit			150	350	425	mA
ΔV_O	Line regulation	V_I = 5.7 to 18 V, I_O = 0.5 mA			4	20	mV
ΔV_O	Load regulation	V_I = 6 V, I_O = 0.5 to 100 mA			3	15	mV
I_d	Quiescent current	V_I = 6 to 18 V, I_O = 0 mA	ON mode		0.5	1	mA
		V_I = 6 to 18 V, I_O = 100 mA			1.5	3	
		V_I = 6 V	OFF mode		50	100	µA
SVR	Supply voltage rejection	I_O = 5 mA, V_I = 7 ± 1 V	f = 120 Hz		76		dB
			f = 1 kHz		71		
			f = 10 kHz		60		
eN	Output noise voltage	B = 10 Hz to 100 kHz			50		µV
V_d	Dropout voltage	I_O = 100 mA			0.2	0.4	V
		I_O = 100 mA, T_J = -40 to 125°C				0.5	
V_{IL}	Control input logic low	T_J = -40 to 125°C				0.8	V
V_{IH}	Control input logic high	T_J = -40 to 125°C		2			V
I_I	Control input current	V_I = 6 V, V_C = 6 V			10		µA
C_O	Output bypass capacitance	ESR = 0.1 to 10 Ω, I_O = 0 to 100 mA		2	10		µF

Refer to the test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified.

Table 9. Electrical characteristics for LE50C

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 7 V		4.9	5	5.1	V
		I_O = 10 mA, V_I = 7 V, T_J = -25 to 85°C		4.8		5.2	
V_I	Operating input voltage	I_O = 100 mA				18	V
I_O	Output current limit			150	350	425	mA
ΔV_O	Line regulation	V_I = 5.7 to 18 V, I_O = 0.5 mA			4	30	mV
ΔV_O	Load regulation	V_I = 6 V, I_O = 0.5 to 100 mA			3	25	mV
I_d	Quiescent current	V_I = 6 to 18 V, I_O = 0 mA	ON mode		0.5	1	mA
		V_I = 6 to 18 V, I_O = 100 mA			1.5	3	
		V_I = 6 V	OFF mode		50	100	µA
SVR	Supply voltage rejection	I_O = 5 mA, V_I = 7 ± 1 V	f = 120 Hz		76		dB
			f = 1 kHz		71		
			f = 10 kHz		60		
eN	Output noise voltage	B = 10 Hz to 100 kHz			50		µV
V_d	Dropout voltage	I_O = 100 mA			0.2	0.4	V
		I_O = 100 mA, T_J = -40 to 125°C				0.5	
V_{IL}	Control input logic low	T_J = -40 to 125°C				0.8	V
V_{IH}	Control input logic high	T_J = -40 to 125°C		2			V
I_I	Control input current	V_I = 6 V, V_C = 6 V			10		µA
C_O	Output bypass capacitance	ESR = 0.1 to 10 Ω, I_O = 0 to 100 mA		2	10		µF

Refer to the test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified.

Table 10. Electrical characteristics for LE80C

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 10 V		7.84	8	8.16	V
		I_O = 10 mA, V_I = 10 V, T_J = -25 to 85°C		7.68		8.32	
V_I	Operating input voltage	I_O = 100 mA				18	V
I_O	Output current limit			150			mA
ΔV_O	Line regulation	V_I = 8.7 to 18 V, I_O = 0.5 mA			5	35	mV
ΔV_O	Load regulation	V_I = 9 V, I_O = 0.5 to 100 mA			3	25	mV
I_d	Quiescent current	V_I = 9 to 18 V, I_O = 0 mA	ON mode		0.7	1.6	mA
		V_I = 9 to 18 V, I_O = 100 mA			1.7	3.6	
		V_I = 9 V	OFF mode		70	140	µA
SVR	Supply voltage rejection	I_O = 5 mA, V_I = 10 ± 1 V	f = 120 Hz		72		dB
			f = 1 kHz		66		
			f = 10 kHz		57		
eN	Output noise voltage	B = 10 Hz to 100 kHz			50		µV
V_d	Dropout voltage	I_O = 100 mA			0.2	0.4	V
		I_O = 100 mA, T_J = -40 to 125°C				0.5	
V_{IL}	Control input logic low	T_J = -40 to 125°C				0.8	V
V_{IH}	Control input logic high	T_J = -40 to 125°C		2			V
I_I	Control input current	V_I = 9 V, V_C = 6 V			10		µA
C_O	Output bypass capacitance	ESR = 0.1 to 10 Ω, I_O = 0 to 100 mA		2	10		µF

5 Typical performance characteristics

Unless otherwise specified, $V_{O(NOM)}$ = 3.3 V.

Figure 4. Dropout voltage vs. output current

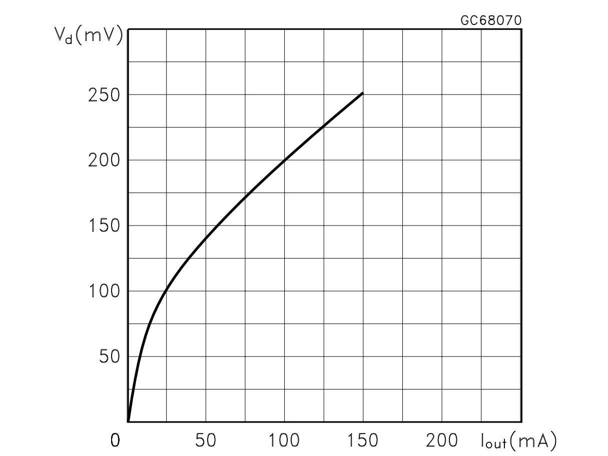


Figure 5. Dropout voltage vs. temperature

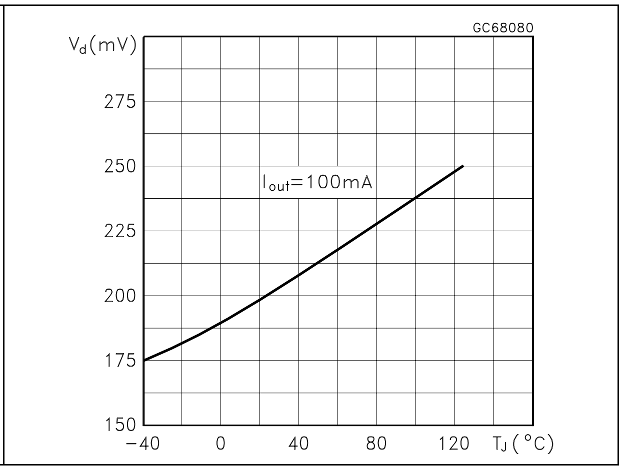


Figure 6. Supply current vs. temperature

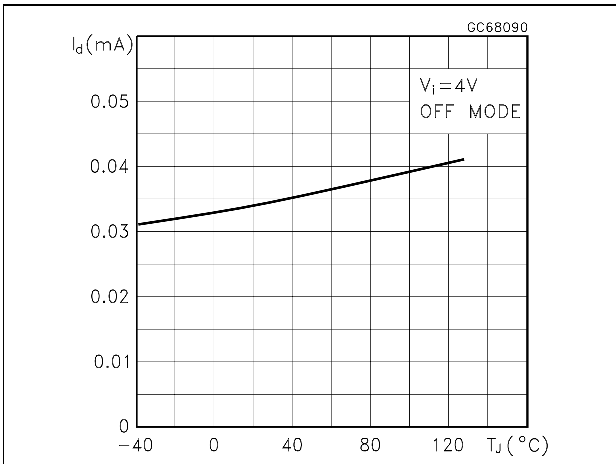


Figure 7. Supply current vs. input voltage

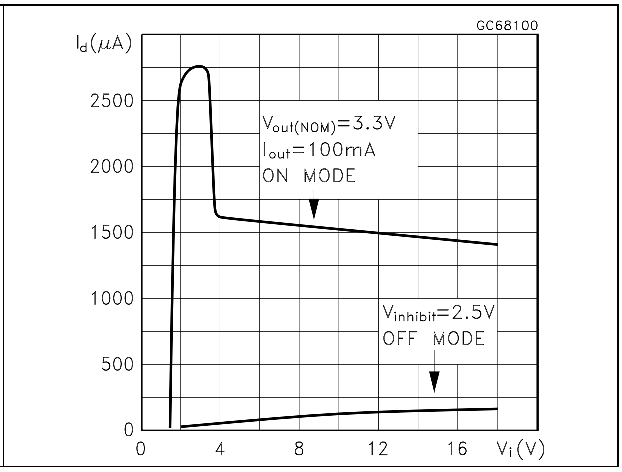


Figure 8. Short-circuit current vs. dropout voltage

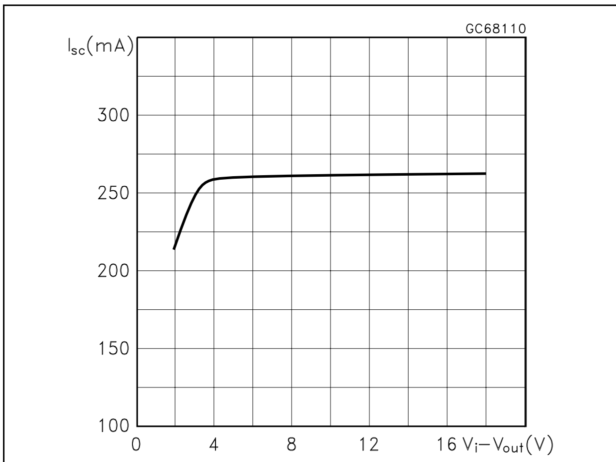


Figure 9. SVR vs. frequency

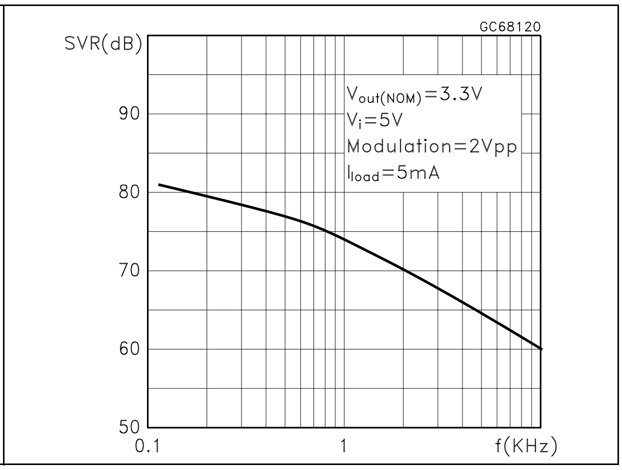


Figure 10. Logic-controlled precision 3.3/5.0 V selectable output

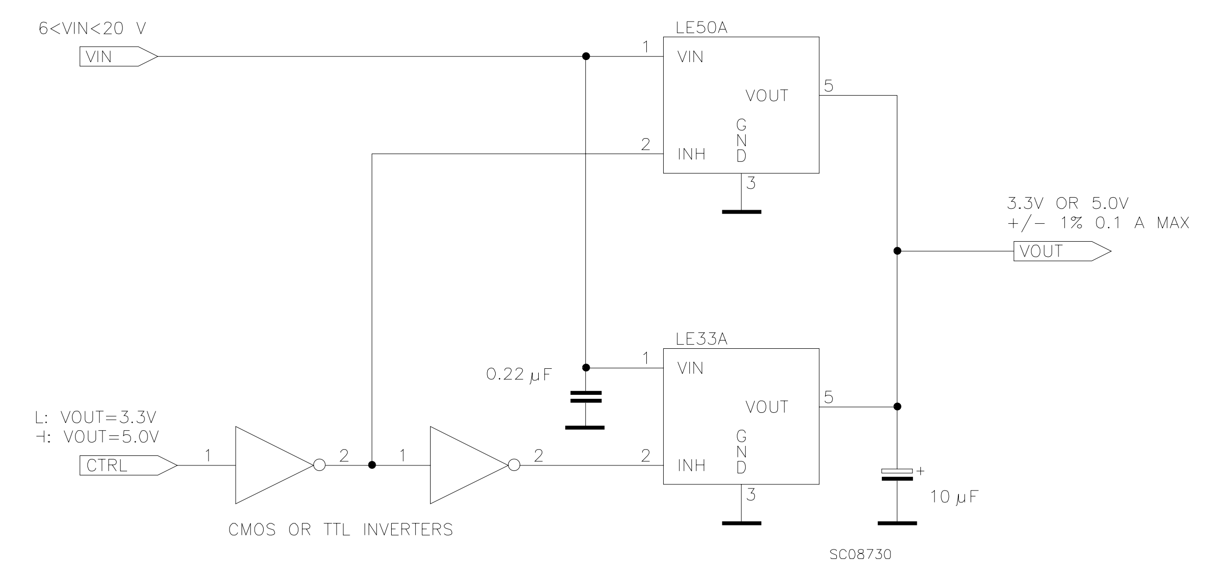


Figure 11. Sequential multi-output supply

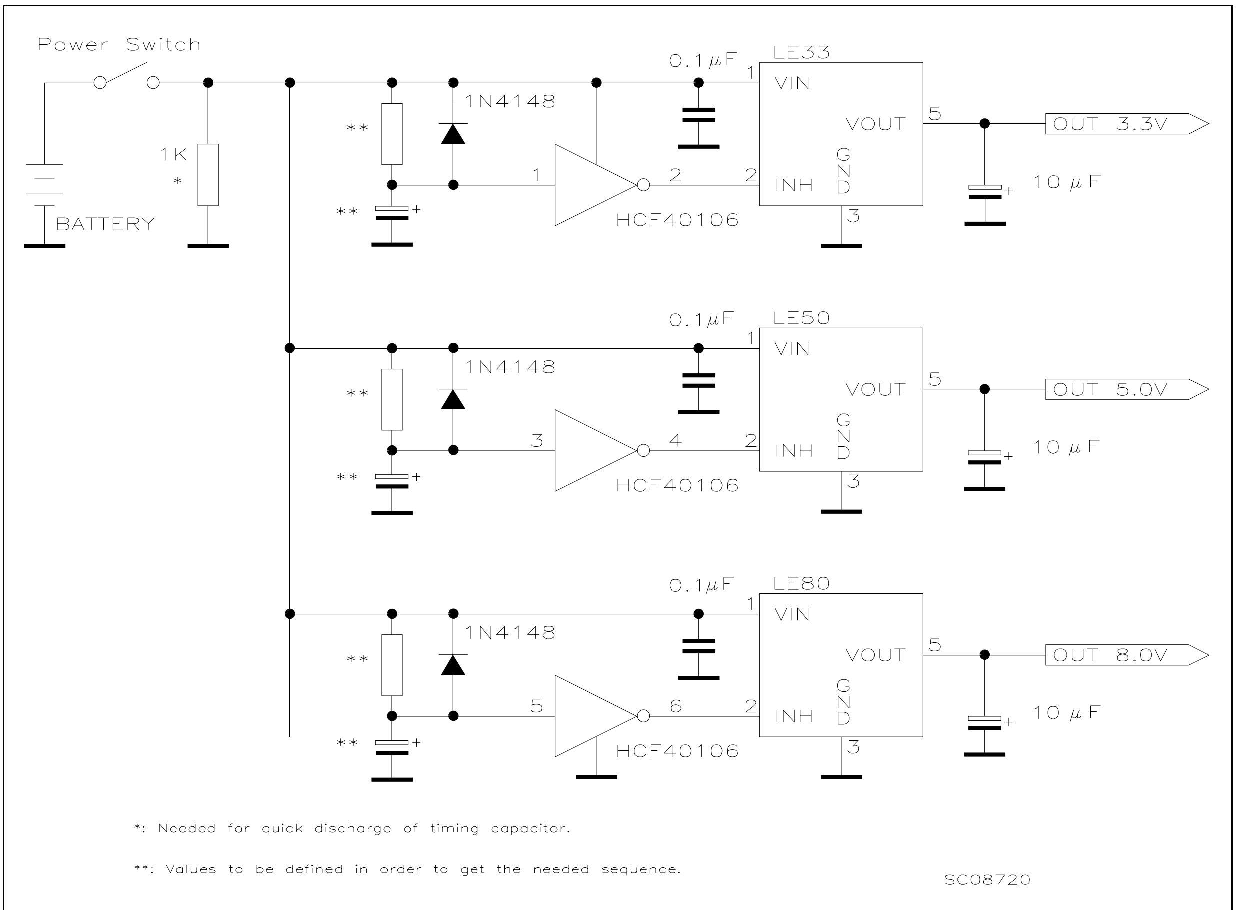


Figure 12. Multiple supplies with ON/OFF toggle switch

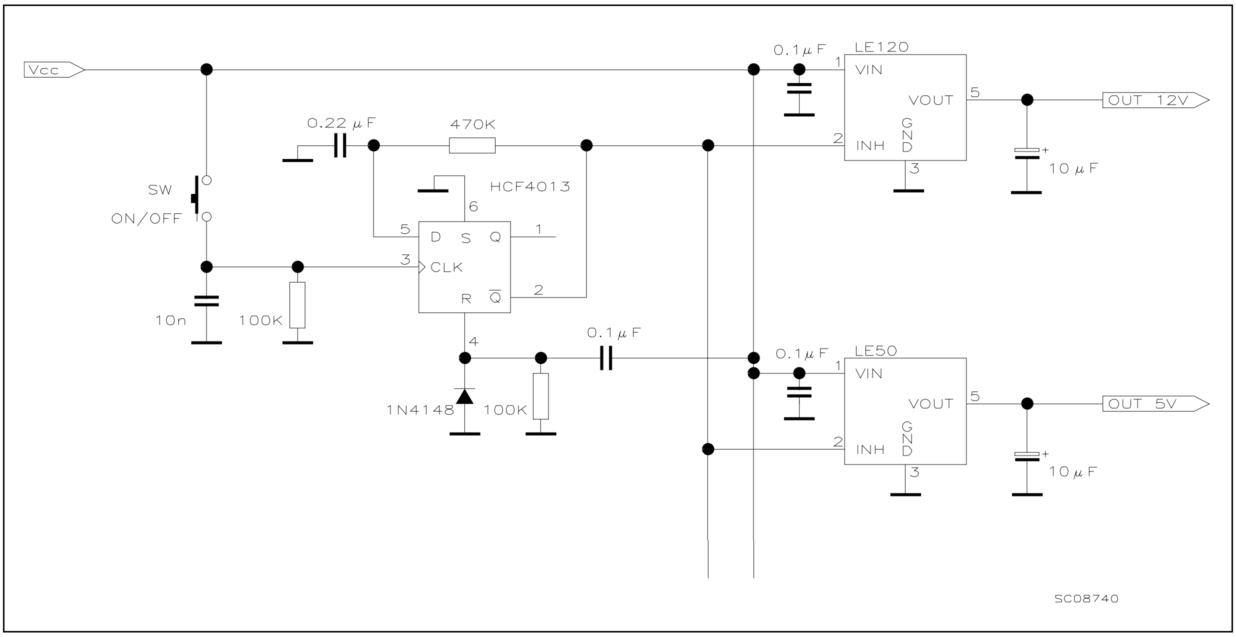
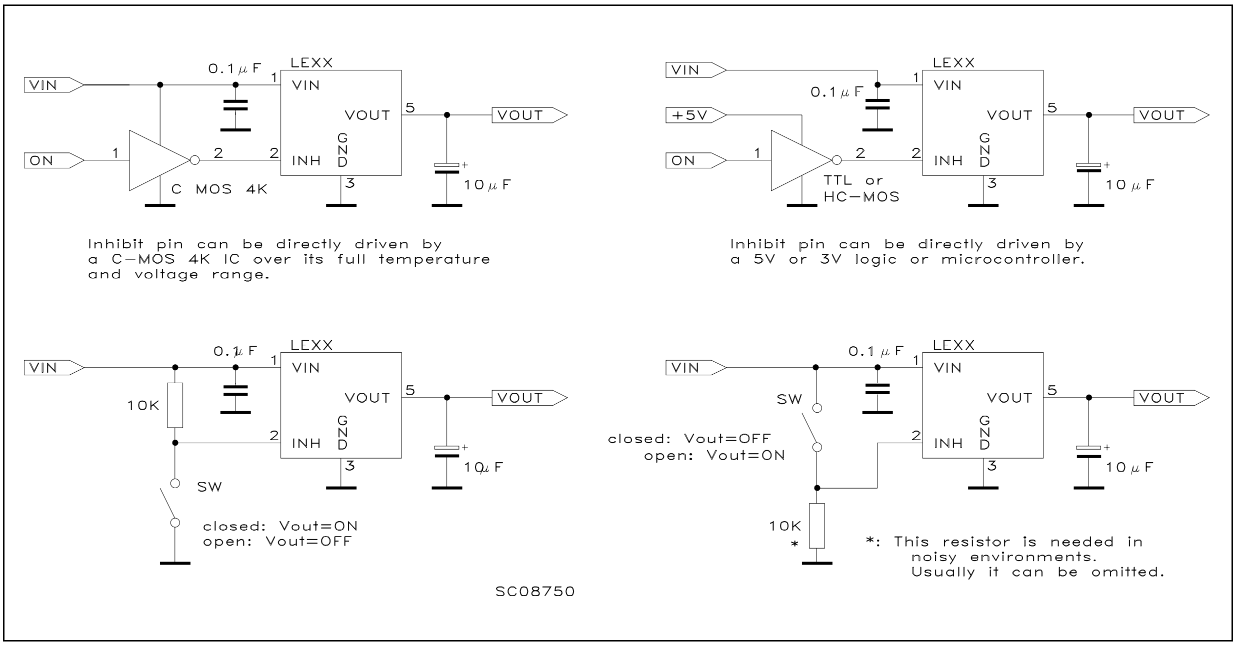


Figure 13. Basic inhibit functions

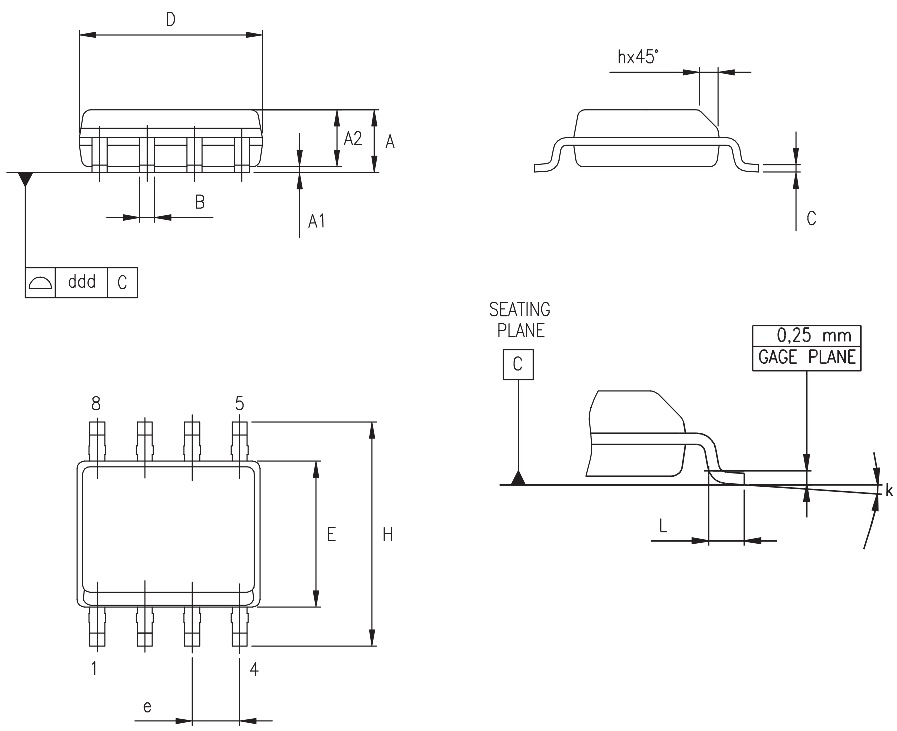


6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

SO-8 mechanical data

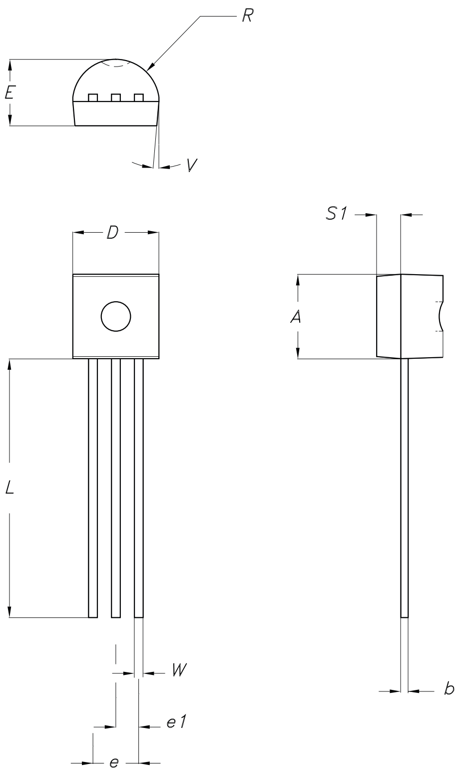
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



0016023/C

TO-92 mechanical data

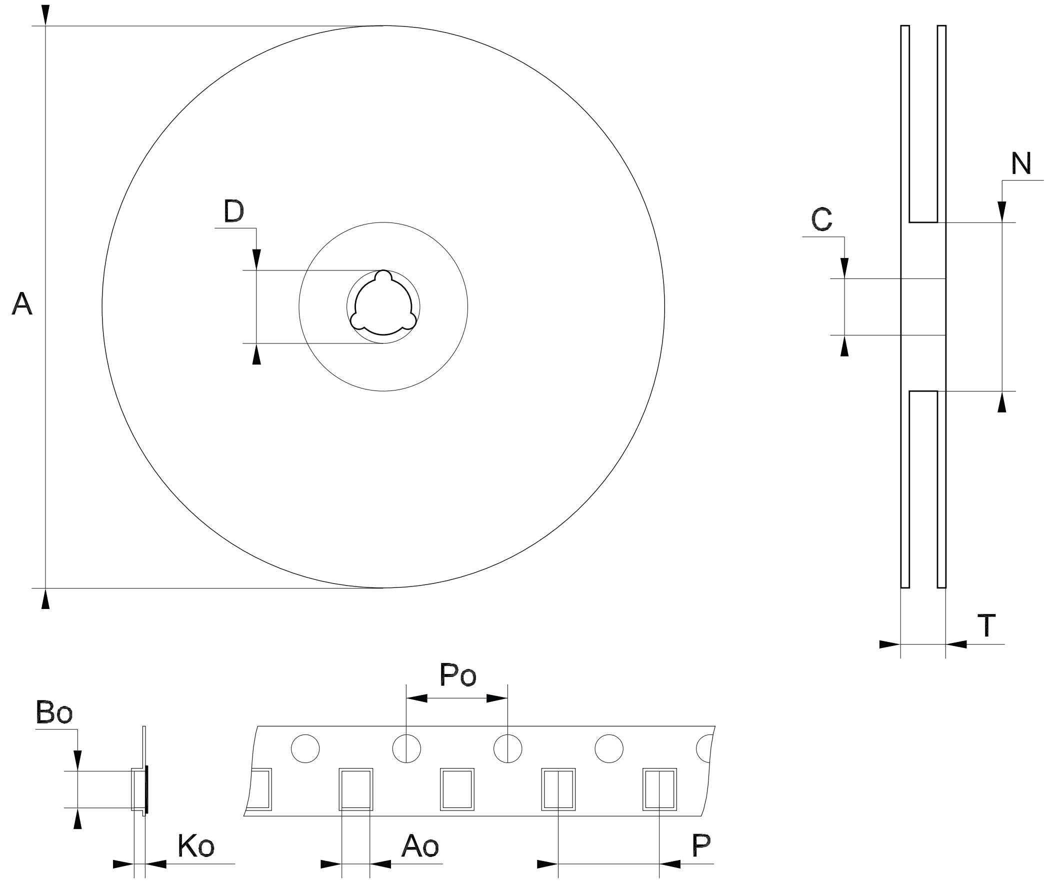
Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.32		4.95	170.1		194.9
b	0.36		0.51	14.2		20.1
D	4.45		4.95	175.2		194.9
E	3.30		3.94	129.9		155.1
e	2.41		2.67	94.9		105.1
e1	1.14		1.40	44.9		55.1
L	12.7		15.49	500.0		609.8
R	2.16		2.41	85.0		94.9
S1	0.92		1.52	36.2		59.8
W	0.41		0.56	16.1		22.0
α		5°			5°	



0102782/D

Tape & reel SO-8 mechanical data

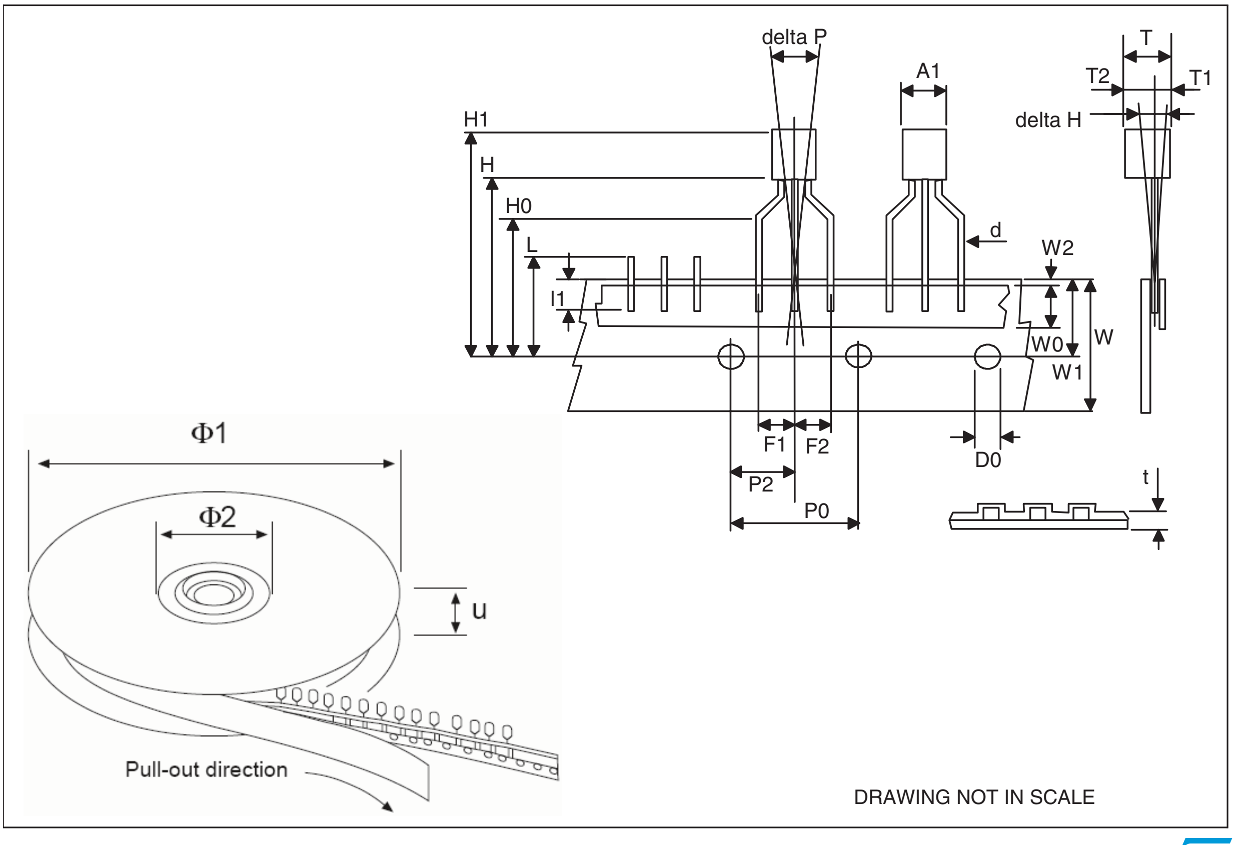
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

Tape & reel for TO-92 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1		4.80			0.189	
T		3.80			0.150	
T1		1.60			0.063	
T2		2.30			0.091	
d		0.48			0.019	
P0	12.5		12.9	0.492		0.508
P2	5.65		7.05	0.222		0.278
F1, F2	2.44	2.54	2.94	0.096	0.100	0.116
delta H		±2			0.079	
W	17.5	18.00	19.0	0.689	0.709	0.748
W0	5.7		6.3	0.224		0.248
W1	8.5		9.25	0.335		0.364
W2		0.50			0.20	
H		18.50	18.70		0.728	0.726
H0	15.50		16.50	0.610		0.650
H1		25.00			0.984	
D0	3.8		4.2	0.150		0.165
t		0.90			0.035	
L1		3			0.118	
delta P		±1			0.039	
u		50			1.968	
Φ1		360			14.173	
Φ2		30			1.181	



7 Revision history

Table 11. Document revision history

Date	Revision	Changes
09-Jul-2004	6	I_O typ. and max. are changed in tab. 24 and 25 - pag. 14.
16-Mar-2005	7	Add Tape & Reel for TO-92 - Note on Table 3.
12-Feb-2007	8	Change value T_{OP} on Table 2.
26-Jul-2007	9	Add Table 1 in cover page.
29-Nov-2007	10	Modified: Table 25.
12-Feb-2008	11	Modified: Table 25.
10-Jul-2008	12	Modified: Table 1 and Table 25.
22-May-2012	13	Updated: *Table 1 on page 1*. Changed: T_A in T_J test conditions from table 4 to table 10.